Micro-Electrode-Cavity-Array (MECA) on a CMOS Chip

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Abstract

- This work represents a CMOS-Based nanopore sensing platform for high resolution readout of nanopore events.
- CMOS integration reduces the overall capacitance of the readout which reduces the overall noise and thus allows detecting of fast and/or small nanopore events.
- The current readout circuit is configurable for different current ranges and bandwidths and optimized for noise suppression. The circuit is divided into four amplifier stages.
- Noise reduction techniques achieve a total integrated noise of only 18 pA_{RMS} in a bandwidth of 1 MHz.
- The ASIC was implemented in a 350 nm standard CMOS technology.
- The ASIC consists of five channels. Four of them are used as a MECA.

Integration of nanopore biosensor and ASIC

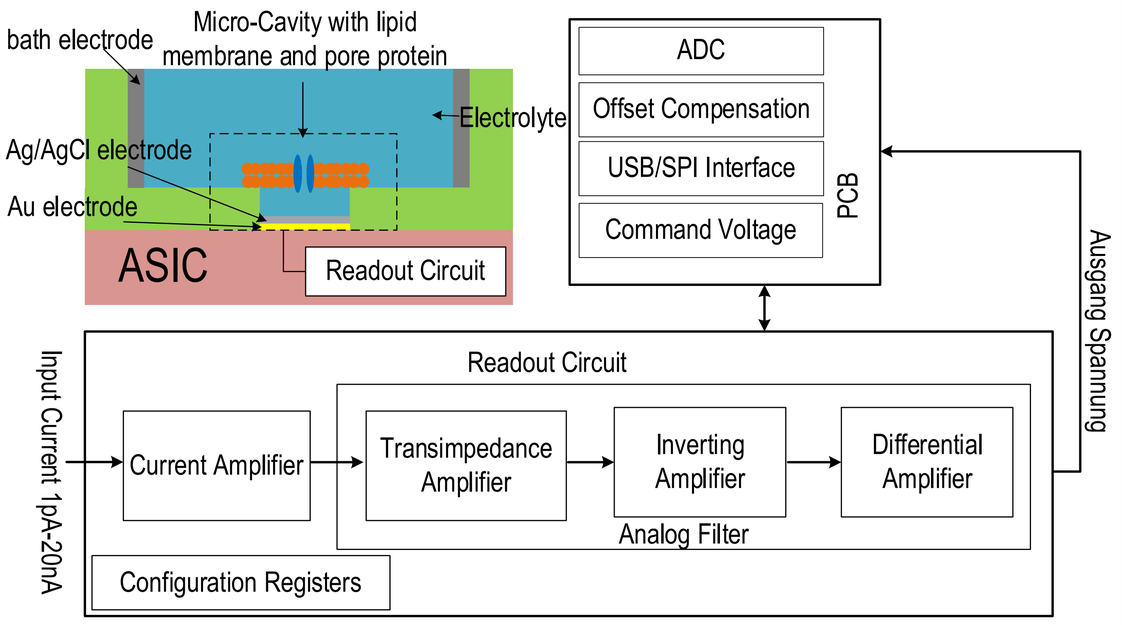


Figure 1: Schematic diagram of the structure of a nanopore sensor on the CMOS integrated readout circuit (ASIC) and external system components.

Circuit diagram, components and specifications of the readout circuit

- The current amplifier (yellow) amplifies the current 100 times.
- The amplified current is converted into a voltage by an integrated transimpedance amplifier (red).
- The output of the TIA is further amplified by the inverting amplifier (green).
- A fully differential output voltage (blue) is generated to reduce the influence of external sources of interference.

Parameter	$OP_{1,2}$	OP_3	OP_4
Input referred voltage noise @1MHZ (nV/√Hz)	2.4	2.84	32
Supply Voltage (V)	±1.65	±1.65	±1.65
Input capacitance amplifier(fF)	750	1600	1440
Input offset Max (mV)	2.2	1.1	14
Gain BW (MHz)	7.3*	12.7**	12**
Phase Margin (deg)	76*	78**	90**
DC gain (dB)	110	117	82
Maximum input CM (mV)	450	700	160
Minimum input CM (mV)	-710	-650	-1650
Supply current (mA)	10	2	0.44

*: at load capacitance of 50pF and feedback factor of 1/7.4
**: at load capacitane of 10pF and feedback factor of 1

Table 1.Summary of OP-Amps specifications.

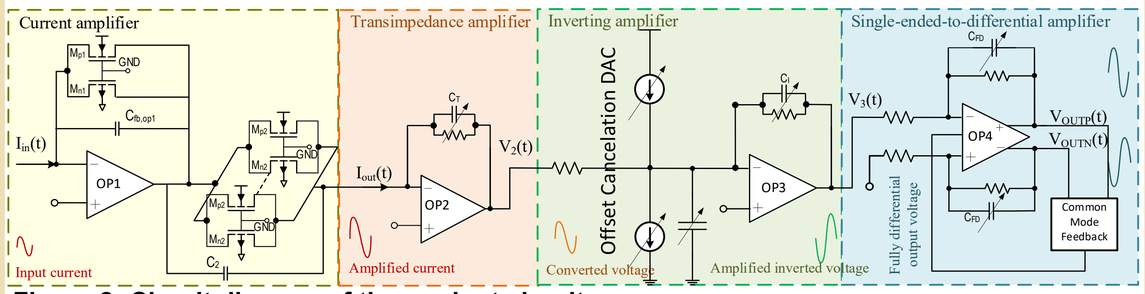
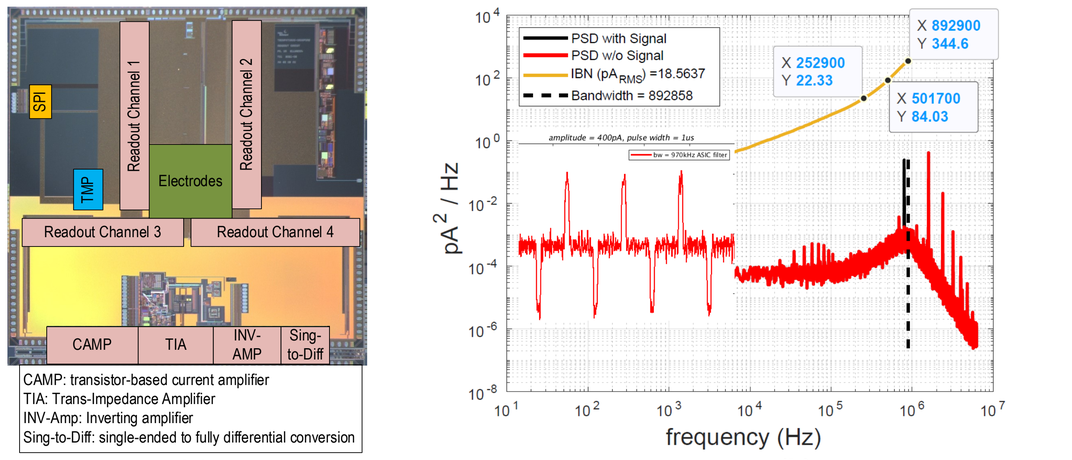


Figure 2: Circuit diagram of the readout circuit.

Measured ASIC Performance



(a) (b)

Figure 4: Measured ASIC Performance. (a) ASIC micrograph. (b) Input referred noise power spectrum density PSD of readout circuit.

CMOS Post Process

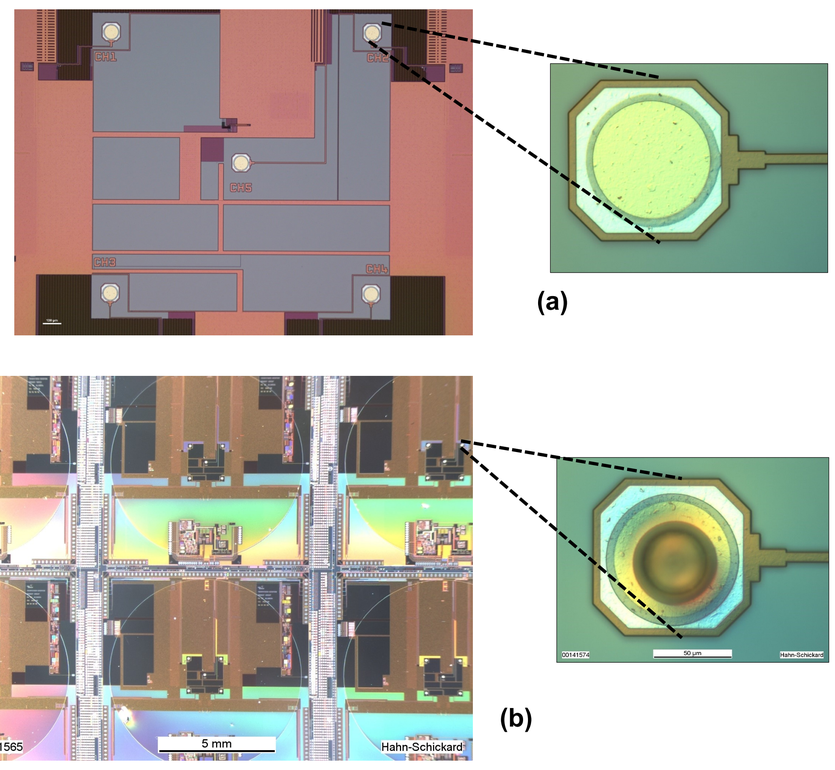
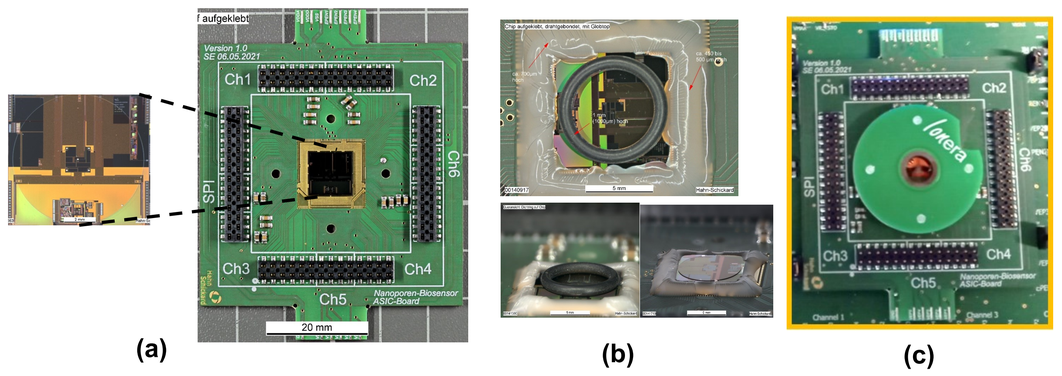


Figure 5: CMOS Post process that includes (a) Gold electrode (b) SU8 cavity (by Ionera Technologies).

Assembly and Packaging



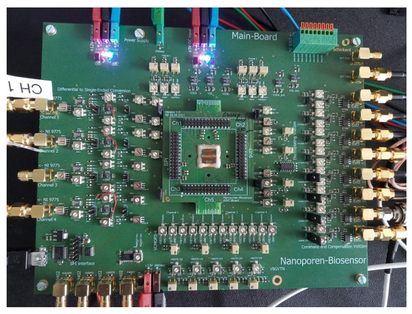


Figure 6: Assembly and Packaging:
(a) ASIC is bonded on ASIC-PCB
(b) Bond wires covered with Epoxy and a seal rubber ring is added
(c) Bath electrode is attached
(d) ASIC PCB is then inserted into an Evaluation PCB.

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